

Process Average Testing (PAT) , Statistical Yield Analysis (SYA) , and Junction Verification Test (JVT)

To enhance the quality control and achieve the zero defect target for automotive grade parts, we need to implement the PAT, SYA, and JVT concept in the production flow.

1 Part Average Testing (PAT)

1.) Definition:

Part Average Testing (PAT) is intended to identify Components that perform outside the normal statistical distribution.

2.) Purpose:

Every part is built with a particular design and process which, if processed correctly, will yield a certain consistent set of characteristic test results. PAT uses statistical techniques to establish the limits on these test results. These test limits are set up to remove outliers (parts whose parameters are statistically different from the typical part) and should have minimal yield impact on correctly processed parts from a well controlled process.

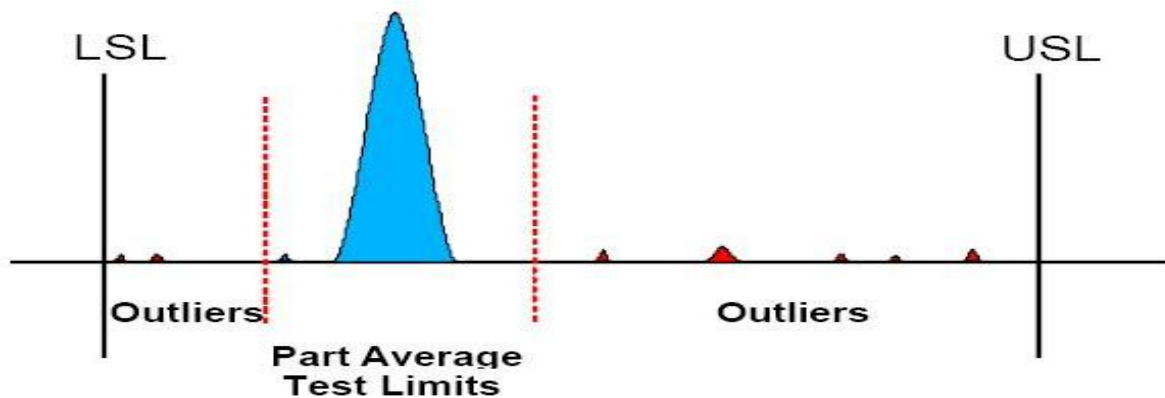


Figure 1 Graphical Representation of Part Average Test Limits and Outliers

History has shown that parts with abnormal characteristics significantly contribute to quality and reliability problems.

3.) Method:

a. Setting The Test Limits

$$\text{PAT Limits} = \text{Mean} \pm 6 \text{ sigma}$$

PAT test limits shall not exceed the device specification limits.

Test limits may be set in either a static or dynamic manner. New PAT limits (both static and dynamic) must be established when wafer level design changes, die shrinks or process changes have been made.

b. Static PAT limits

The static limits are established based on an available amount of test data and used without modification for some period of time.

Sample Size:

Package parts: 30 pass parts x at least 6 lots.

Wafer level: 30 pass dies from at least 5 die located x at least 6 lots.

When data from six lots is not available, data from characterization lots may be used. This data shall be updated as soon as production data is available.

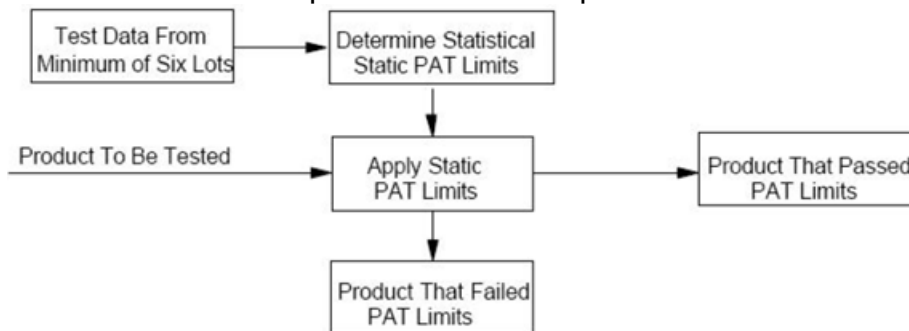


Figure 1 Determining Static PAT Limits

The first 6 months: PAT test limits shall be reviewed and updated as required using current data of production or the last 8 lots. Older data shall not be used.

After 6 months: The static PAT limits shall be reviewed and updated as needed on a quarterly (every 3 month) basis.

c. Dynamic PAT limits

The dynamic test limits are based on the static limits, but are established for each lot and continually change as each lot is tested.

Sample Size: Same as Static PAT limits

The dynamic limits shall not exceed the static limits.

Dynamic PAT can provide tighter limits without causing rejection of good parts because it does not have to consider the lot -to-lot variation that is part of Static PAT Limits.

This analysis establishes new tighter test limits for that particular lot (or wafer) and removes additional outliers.

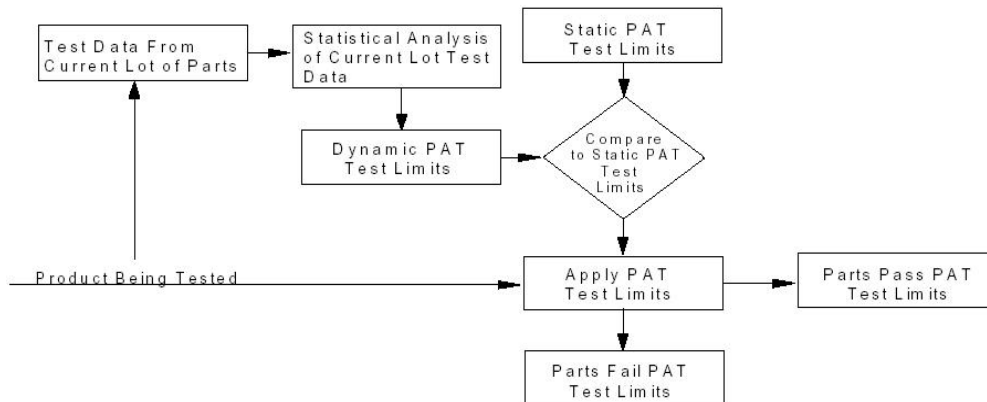


Figure 2 Determining Dynamic PAT Limits

The lot of parts being tested must be held in a manner that allows the outliers to be removed after the test limits for the lot have been calculated and applied.

4.) Application on electrical tests

Any electrical parameter with a Cpk greater than 2.0 ($CPK = 2.0 = 6\sigma$) is considered a candidate for implementation.

PAT limits should be used for all electrical tests if possible, but shall be established for at least the important characteristics as below :

- a. Junction Verification Test (JVT) - Pin Leakage Test
- b. Standby power supply current (IDD or ICC)
- c. IDDQ: tested with at least 70% transistor-level coverage (TLC). If the device design is not capable of being tested, then this requirement does not apply.
- d. Output breakdown voltage (BVCEs or BVDSS)

Output leakage (ICES or IDDS), measured at 80% of the breakdown voltage value

Output current drive (IOUT) and output voltage levels (VOUT)

e. Additional tests:

- 1) Voltage Stress Test (Vs)
- 2) Low Level Input Current (IIL)
- 3) High Level Input Current (IIH)
- 4) Propagation Delay Or Output Response Time
- 5) Rise/Fall Times
- 6) Low Level Output Voltage (VOL)
- 7) High Level Output Voltage (VOH)
- 8) Extended Operating Tests

Extended operating tests are tests beyond the device specification requirements intended to increase the effectiveness of PAT. The following are some examples of extended operating tests: a.) voltage stress b.) low voltage operation c.) high voltage operation d.) operating

frequencies above specification requirements e.) operating frequencies below specification requirements on power devices, demonstration of safe operating capability at 60% of safe operating limit, followed by leakage testing, etc.

The only restriction on these tests is that it must be demonstrated that the test does not adversely affect the reliability of the part.

2 Statistical Yield Analysis (SYA)

1.) Definition:

Statistical Yield Analysis (SYA) identifies lots of components that yield abnormal distributions, or contain abnormal failure characteristics.

2.) Purpose:

Utilizes statistical techniques to identify a wafer, wafer lot, or component assembly lot that exhibits an unusually low yield or an unusually high bin failure rate. Experience has shown that wafer and component assembly lots exhibiting these abnormal characteristics tend to have generally poor quality and can result in insignificant system reliability and quality problems that impact the customer.

3.) Method:

a. 2 ways: statistical yield limits (SYL) and statistical bin limits (SBL) results. Both use test limits based on Part Average Testing (PAT) Limits.

b. Sample Size: Collect data from at least six lots and determine the mean and sigma value for the percentage of devices passing per lot and the percentage of devices failing each bin-out per lot

Early in production of a part, when data from six lots is not available, data from characterization/matrix lots may be used. This data shall be updated as soon as production data is available

c. The first 6 months: This early data shall be reviewed and updated using current data at least every 30 days. The current data used shall include the data available since the last update or at least the last 8 lots. Older data shall not be used

After 6 months: the limits shall be updated on a quarterly (every 3 months) basis

d. Setting the value for SYL and SBL

$$SYL_1 = \text{Mean} - 3 \text{ Sigma}$$

$$SBL_1 = \text{Mean} + 3 \text{ Sigma}$$

$$SYL_2 = \text{Mean} - 4 \text{ Sigma}$$

$$SBL_2 = \text{Mean} + 4 \text{ Sigma}$$

e. Disposition: Any lot that fall below SYL1 or exceed SBL1 shall be held for engineering review. In addition, lots that fall below SYL2 or exceed SBL2 may be impounded and require customer notification before release. Analysis shall be performed on failures to determine the failure mechanism causing these abnormal failure rates.

f. Records: The supplier shall maintain records on all lots that fall below SYL1 or exceed SBL1. This data shall include the root cause for the yield problem and corrective action taken to prevent reoccurrence of the problem. It should also include any special testing or screens that were performed on lot and the customer that approved the shipment of the parts in question.

4.) Customer Notification

a. Supplier shall have determined the failure mechanism and, based on his experience, determine the corrective action required to prevent a reoccurrence of the condition in future product. The supplier shall also present a plan for additional tests and screens which could provide the user with reasonable certainty that the product he receives will be at least equal to normal product.

b. The customer reserves the right to reject material that falls below SYL2 or exceeds SBL2 if the supplier data does not satisfy his concerns about the quality. The parts from the lots falling below SYL2 shall not be supplied to distributors as meeting AEC - Q100 if the supplier does not know who the customer is and customer approval can not be obtained.

3 Junction Verification Test (JVT)

1.) Definition:

Junction Verification Test (JVT) is also called "Pin leakage Test". This test will verify that the semiconductor device pins have normal junction characteristics with respect to substrate and with respect to VDD in the case of CMOS components.

2.) Purpose:

Junction Verification Test (JVT) is used to identify IC which have wounded electrical junctions or are susceptible to EOS or a latch up condition and, perform outside the normal statistical distribution.

3.) Method:

Use the following measurement approach to establish the PAT limits for pin leakage.

a. With all pins grounded except the pin under test (PUT):

1) Force -10mA into each pin, measure the forward biased junction voltage (V F1).

2) For CMOS, also force +10mA into each pin, measure the forward biased junction voltage (VF1).

3) Test VDD (VCC) separately with respect to the substrate using -10mA, measure the forward biased junction voltage (VF2).

- 4) Statistically analyze this data to determine the mean for VF1 and VF2.
- b. With all pins grounded except the pin under test (PUT), and using the VF1 and VF2 values determined above, measure the leakage current:
- 1) Apply -0.8 VF1 (80% of forward bias voltage) to each pin, measure the leakage current.
 - 2) For CMOS, also apply +0.8 VF1 to each pin, measure the leakage currents.
 - 3) Apply -0.8 VF2 to VDD (VCC), measure the leakage current.
 - 4) Statistically analyze this data to determine the leakage current PAT limits.
- c. After the conclusion of the final ATE test and following powering down, perform this test method to detect any possible damage that could have occurred during testing.